

Serial No. 09/710,057

Amendment dated January 8, 2004

Response to Notice of Non-Compliant Amendment dated February 3, 2004

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**Amendments to the Specification:**

Please amend the Specification as follows:

Page 15, line 18, delete the blank line after "Ser. No." and replace it with "09/709,855"; and

line 19, delete " , now U.S. Pat. No. \_\_\_\_\_," so that the paragraph reads as follows:

The operation of the mode controller 220 is described in detail in copending patent application, U.S. Patent App. Ser. No. [\_\_\_\_\_]09/709,855, filed 10.11.00 (10 November 2000) (docket number 62061.0103)[ ~~, now U.S. Pat. No. \_\_\_\_\_,~~] entitled "Method and Apparatus for Static Test Pattern Generation Within a Dynamic Pseudo-random Test Program Generation Framework," (hereinafter, the "Static/Dynamic Generator Patent") which is incorporated by reference into this specification for all purposes. In addition, the Static/Dynamic Generator Patent also describes the use of templates 214 and the operation of the test generator in both sequential mode and dynamic mode, and details regarding templates and the test generator operating modes are not repeated herein. While the present invention makes use of templates as described in the Static/Dynamic Generator Patent, the special sequential operating mode of the test generator described in the Static/Dynamic Generator Patent does not apply to the present invention. For the purposes of this disclosure, the reader should assume that the test generator is always operating in dynamic mode.

Page 16, line 22, delete the blank line after "Ser. No." and replace it with "09/709,801", and

Page 17, line 2, delete the blank line after "Pat. No." and replace with "6,606,721" so that the paragraph reads as follows:

Returning to FIG. 3, information from the user preference queue 206, the resource-related data structures 210, the rules table 209, and existing templates 214 is combined in the instruction packer 208 to create sequences

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of instructions or groups of parallel instructions for generation and simulation. As explained in further detail below, the resource-related data structures 210 are data structures that are created, maintained, and updated to track the actual and/or predicted past state, present state, and future state of selected system resources. In this specification the term "system resources" is defined to include both architectural resources and conceptual resources. Architectural resources include resources like the architectural state of the processor (as defined by the state of specific registers), other registers, the load/store buffer, and the like. The term "conceptual resources" refers to resources that may not actually exist within the architectural state of the machine under test, but instead represent a simple way to represent complex interactions, such as whether or not a branch instruction is pending, or the usage of various execution units over time, or estimated bus traffic at a particular point in time. Practitioners of the present invention may wish to adopt the tracking methodologies and approaches described in detail in copending patent application, U.S. Patent App. Ser. No. [[ ]]09/709,801, filed 10.11.00 (10 November 2000) (docket number 62061.0106), now U.S. Pat. No. [[ ]]6,606,721, entitled "Method and Apparatus that Tracks Processor Resources in a Dynamic Pseudo-Random Test Program Generator," (hereinafter, the "Resource Tracking Patent") which is incorporated by reference into this specification for all purposes, to identify system resources appropriate for tracking and to track those resources.

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